High-density PCB assemblies for space applications: from evaluation to qualification

15-18 October 2024
ESA/ESTEC, Noordwijk, The Netherlands

Maarten Cauwe[(1)], Chinmay Nawghane[(1)], Marnix Van De Slyeke[(2)], Alexia Coulon[(3)], Thibault André[(3)], Stan Heltzel[(4)]

[(1)] imec and Ghent University
Technologiepark 126, Zwijnaarde, Belgium
Email: Maarten.Cauwe@imec.be

[(2)]Group ACB
Vosmeer 3, Dendermonde, Belgium

[(3)]Thales Alenia Space Belgium
Rue Chapelle Beaussart 101, Mont-sur-Marchienne, Belgium

[(4)]ESA-ESTEC
Keplerlaan 1, Noordwijk, The Netherlands

INTRODUCTION

High density interconnect (HDI) printed circuit boards (PCBs) and associated assemblies are essential to allow space projects to benefit from the ever increasing complexity and functionality of modern integrated circuits such as field programmable gate arrays (FPGAs), digital signal processors (DSPs) and application processors. Increasing demands for functionality translate into higher signal speeds combined with an increasing number of inputs and outputs (I/Os). To limit the overall package size, the contact pad pitch of the components is reduced. The combination of a high number of I/Os with a reduced pitch places additional demands onto the PCB, requiring the use of laser drilled microvias, high aspect ratio core vias and small track width and spacing. While the associated advanced manufacturing processes have been widely used in commercial, automotive, medical and military applications; reconciling these advancements in capability with the reliability requirements for space remains a challenge.
Two main drivers are commonly identified for HDI PCBs: (1) the small pitch and high number of I/Os of key components and (2) the increasing performance of these components resulting in high-speed signal lines on the boards. The use of microvias allows to reduce the length of the signal path, improving both signal integrity and power integrity. Critical nets may suffer from crosstalk due to the dense routing within the fanout. The routing of differential pairs in between the pins of a 1.0 mm pitch component requires fine line widths and spacing. Differential pair routing in between the core vias for 0.8 mm pitch components is not always possible. The pairs need to be split within the fanout area and the effect on signal integrity will depend on the length of the split. The change in width on single-ended nets, as well as a change in the spacing and/or trace widths of a differential pair, will cause an impedance discontinuity. Choosing the appropriate layer build-up and via types will thus improve both route-ability and signal integrity.
At the start of the project in 2018, a stakeholder workshop was organized at ESTEC in order to derive the requirements for HDI PCBs in space projects. Workshop participants were primes, equipment manufacturers, space agencies, ESA qualified PCB manufacturers, ESA technical officers and independent conductive anodic filament (CAF) experts. During the workshop, a decision was made to differentiate between “basic HDI technology”, intended for immediate qualification, and “complex HDI technology”, covering more advanced technology parameters. Based on the feedback of the stakeholders, a set of HDI technology parameters was defined, which are described in the next section. The basic HDI technology parameters cover the short-term need for increased functionality at an acceptable manufacturing risk level, without compromising reliability. Large FPGA components, based on 1.0 mm pitch ceramic column grid array (CCGA) packages with up to 1752 pins, are the primary drivers for the basic HDI technology (e.g. Xilinx Virtex 5QV, Microchip RTG4). In addition, the basic HDI technology is compatible with area array devices (AAD) with 0.8 mm pitch and a few hundred I/Os (e.g. ceramic ball grid arrays (CBGA) used in Teledyne e2v analogue-to-digital converters). Other driving components are small passives (0402 chip components) and fine-pitch lead frame components (e.g. quad flat packages (QFPs) with 0.5 mm pitch) when routing space is limited. High-density connectors (e.g. Nano-D type with 1.27 mm pitch) also drive HDI requirements. At the time of the workshop, data transfer rates on HDI PCBs for near-term space projects were mostly below 5 Gbps. Polyimide remains the material of choice for HDI PCBs in space applications, in a single-sequence core construction with two levels of copper-filled microvias. Two levels of microvias is considered sufficient to route the AADs with 0.8 mm and 1.0 mm pitch, covering the functional requirements for these projects. To minimize the reliability risk, the microvias are staggered with respect to each other and to the core via.

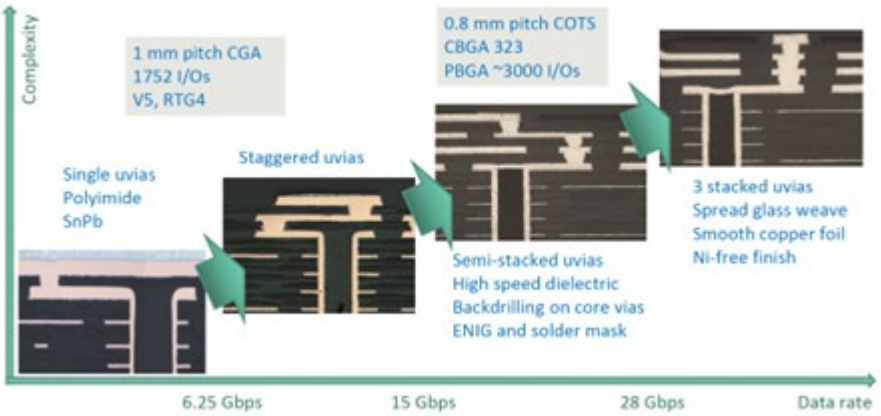

Fig. 1. HDI PCB technology development roadmap from basic HDI over complex HSI towards high-speed HDI

In more advanced projects envisioned at the time of the workshop, components have up to 2000 to 3000 I/Os and use AADs with 0.8 mm and 1.0 mm pitch. These will likely be non-hermetic polymer-based packages (e.g. plastic BGAs), as a package size of 45 mm x 45 mm for ceramic packages is the limit in terms of CTE mismatch [1]. A further reduction in pitch to 0.5 mm pitch is expected for low I/O count (200 – 300) and for memory devices. Data rates are projected to increase up to 15 Gbps and power dissipation is expected to rise to 12 – 15 watts. The increased number of I/Os and reduced pitch translate into the need for three levels of microvias in the complex HDI technology. The microvia configuration of choice is the semi-stacked option consisting of two stacked microvias plus one staggered microvia. Stacking three levels of microvias was considered a reliability risk at the time. To accommodate the need for RF and high-speed digital applications, a high-speed base material is included in the complex HDI technology evaluation.
Solder mask and a flat surface finish compatible with fine-pitch components are considered a requirement for the complex HDI technology. A surface finish without Ni has benefits with respect to RF performance and avoids the creation of more brittle Ni-Sn intermetallic [2]. Ni-free options are either still rare (EPIG, ISIG) or not compatible with the fine spacing and planarity requirements of HDI components (reflowed SnPb). Electroless Nickel Immersion Gold (ENIG) is considered more suitable for large AAD components, while adding an additional electroless palladium layer makes the ENEPIG finish suitable for wire bonding [3].
Looking back at this assessment at the start of the project, most of the considerations remain valid. It should be noted, however, that the relevance of the complex HDI technology has diminished. The increased routing density is mainly applicable to advanced components that have additional requirements with respect to data speeds and power. These components required the use of high-speed base materials instead of polyimide and imposed additional design restraints to ensure signal and power integrity. Such components are driving the high-speed HDI technology that is developed as part of a follow-up activity.

TECHNOLOGY PARAMETERS

The HDI technology parameters for basic and complex HDI can be found in Table 1. The fine-pitch conductor line width and spacing on the non-plated inner layers are driven by the need for routing differential pairs in between the pads of two neighbouring core vias. Reducing the conductor line width and spacing allows the use of a larger pad diameter to achieve the requirement of more than 25 µm annular ring (as manufactured). The possible yield loss on inner-layer manufacturing is offset by the lower risk of misregistration after lamination.
Two levels of microvia in staggered configuration is not considered a risk by the PCB manufacturers and is thus selected for the basic HDI technology. The complex HDI technology uses three levels of microvias. Microvias for all HDI technologies are copper-filled.
Cleanliness remains critical for HDI PCBs. A single prepreg sheet is still considered risky for the introduction of contamination (FOD - foreign object debris), most notably during the lay-up process. Furthermore, the use of two sheets of prepregs in the microvia layers provides better resin flow and, consequently, better dielectric thickness control. Two sheets of prepreg are to be applied on all layers in the basic HDI technology. The use of a single sheet of prepreg for the microvia layers is evaluated in the complex HDI technology.
To improve the interconnect stress test (IST) endurance and the overall reliability, the drill diameter of the core vias for the basic HDI technology is increased from 300 µm agreed at the workshop to 350 µm. A 350 µm drill diameter for the 20-layer basic HDI construction (core thickness of about 2.35 mm) translates to a maximum aspect ratio of 7 instead of 8. The increased core via drill diameter makes it more challenging to control the dielectric thickness when the core vias are filled with the resin of the prepregs in the microvia layers. Via plugging is thus needed, which can also improve the reliability of the core via. Similarly, for future AADs with high pin count (> 2000), the number of core vias will be too high to allow for prepreg filling. Via plugging is used for the complex HDI technology as well. A thin cap plating (5 µm thickness) is required to prevent potential dielectric cracks from propagating into the microvia layers. An additional advantage of plugging the core vias is the possibility to plate thicker copper inside the holes without impacting the thickness of the surface copper (due to the planarization step). The required copper thickness inside the core via for the

basic HDI technology is increased to 35 µm on average and 30 µm minimum. As concluded in an IST study (see relevant section), all non-functional pads are removed on core vias. Together with back drilling of core vias, this was foreseen for the complex HDI technology to improve signal integrity.
Combining flex layers with rigid HDI PCB technology allows avoiding cables for interconnection from board to board. This is an advantage in space-limited equipment designs. Including flex layers has an impact on manufacturing yield due to the alignment challenges. In addition, IST performance is impacted negatively and electromigration failures have been observed. These three risk factors motivate the choice of not including rigid-flex technology in the basic and complex HDI technology.
Solder mask is a requirement for the complex HDI technology. Other surface finishes (ENIG, ENIPIG, ENEPIG, and EPIG) are of interest, but the focus of the project is not to evaluate alternative surface finishes. The complex HDI technology was evaluated with both ENIG and ENEPIG (one finish per base material). The preference of the PCB manufacturer was to combine ENIG with Ventec VT-901 and ENEPIG with Megtron 6.

Table 1. HDI technology parameters for basic and complex HDI technology. *Parameters highlighted in blue were revised after the initial qualification trial for the basic HDI technology to improve core via endurance*

HDI techn. parameter	basic HDI	complex HDI
Conductor width and spacing, as-designed	Fine pitch on non-plated inner layers (17 µm Cu): 70 µm line width and 70 µm spacing	Fine pitch on non-plated inner layers (12 µm Cu): 50 µm line width and 50 µm spacing
Configuration of microvias	Two levels of microvias, staggered, Cu filled, 175 µm diameter	Three levels of microvias, Cu filled, 125 µm diameter; Semi-stacked inside configuration
Number of layers	≤ 20	≤ 26
HDI layers construction	Staggered to core, two sheets of prepreg.	Staggered to core, one sheet of prepreg.
Aspect ratio of core vias	≤ 7	≤ 9
PCB thickness	2.8 mm	Approx. 3 mm
Filling medium for core vias	Via plugging (with cap plating)	Via plugging (with cap plating)
Construction of core	Single sequence, 350 µm drill diameter and 650 µm pad diameter for core vias.	Single sequence, 250 µm drill diameter and 550 µm pad diameter for core vias.
Back drilling	No	Back drilling on core
Presence of non-functional pads	Full pad stack removed on core vias	Full pad stack removed on core vias
Dielectric material	Polyimide (Ventec VT-901)	Polyimide (Ventec VT-901)
RF material	No	Yes (Panasonic Megtron 6)
Surface finish and solder mask	SnPb, no solder mask	ENIG or ENEPIG with solder mask
Core via Cu thickness	35 µm average, 30 µm minimum	25 µm average, 20 µm minimum

DESIGN RULES

Based on the technology parameters and the lessons learned during the qualification of the basic HDI technology and the evaluation of the complex HDI technology, a set of design rules is put forward. These design rules serve as input for future updates of ECSS-Q-ST-70-12C [4].
Following the weak microvia interface issues, the recommended aspect ratio for high-quality microvias is 0.66 to 0.75. Both the dielectric thickness and the base copper foil thickness need to be considered for the calculation of the microvia aspect ratio. To minimize variations in dielectric thickness, the microvia layers should be assigned as plane layers. This also ensures the best control over the plated copper thickness. The prepreg construction for the microvia layers should be selected based on the worst-case copper thickness on the plated layers. The basic HDI qualification test vehicle applied 12 µm base copper foil on the microvia layers in order to achieve a total copper thickness of around 40 µm. A 2x 106 prepreg construction was used to ensure an as-manufactured minimum dielectric thickness of 60 µm on the microvia layers (see next section for more details).
The design rules for placement of the staggered microvia is tangency of the pads (centre-to-centre distance between two microvias of 350 µm for basic HDI and 275 µm for complex HDI). The same applies for the microvia and the core via (centre-to-centre distance between microvia and core via of 500 µm for basic HDI and 412.5 µm for complex HDI). This design rule ensures that, even for worst-case misregistration, the microvia drill will not overlap with the adjacent microvia or core via drill. Note that the tangency of the microvia with respect to the core via requires a minimum spacing of 100 µm on the (plated) outer layers of the core in the basic HDI construction.

During the project, testing and modelling indicated that microvia placement superimposed to the core via results in higher strains. The recommendation is to place the pad of the external microvia tangent to the pad of the core via on the layer below, similar to the design rule for the internal microvia. If superimposing microvias above the core via cannot be avoided, concentric placement is advised.
The required track width and spacing on the signal layers in the core (non-plated inner layers) is defined by the need for differential pair routing in between the core vias. The available space is determined by the component pitch and the required core via pad size. This pad diameter is a compromise between annular ring requirement and linewidth & spacing specifications. The preference is to keep the annular ring at 150 µm (as-designed), resulting in a pad size of 650 µm for a drill diameter of 350 µm in case of the basic HDI technology. The as-designed linewidth and spacing to allow differential pair routing in the fanout area of a 1.0 mm pitch component is 70 µm (650/2 + 5x 70 + 650/2 = 1.0 mm, Fig. 2 – left). Differential pair routing for 0.8 mm pitch components is not possible with the basic HDI. The complex HDI both reduces the core via drill diameter (250 µm with a pad diameter of 550 µm) and the minimum line width and spacing (50/50 µm) to enable differential pair routing for 0.8 mm pitch components (550/2 + 5x 50 + 550/2 = 0.8 mm, Fig. 2 – right).

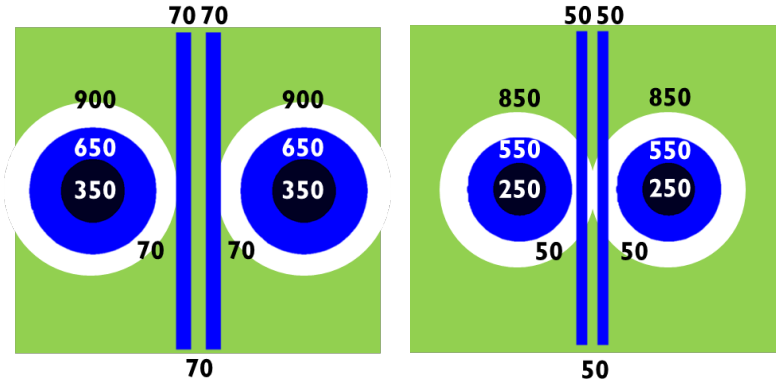

Fig. 2. Differential pair routing for a 1.0 mm pitch component in the basic HDI technology (*left*) and for a 0.8 mm pitch component in the complex HDI technology (*right*). *Blue represents the signal layer and green the reference plane layer*

QUALIFICATION OF BASIC HDI TECHNOLOGY

Following the definition of the basic HDI technology parameters, a qualification test vehicle (QTV) with a representative PCB and appropriate test structures was designed. The QTV was submitted to the qualification test flow for HDI technology, as defined in ECSS-Q-ST-70-60C [5]. Unfortunately, this initial qualification attempt for the basic HDI technology was not successful. Microvia failures were observed during IST. Cracks in the core vias are detected after group 6 testing in both the 0.8 mm and 1.0 mm pitch fanout. Similar failures were observed at other manufacturers as well. An investigation into the contributing factors to core via reliability was launched. Based on the outcome of this investigation, the technology parameters for the basic HDI technology were revised (main changes highlighted in blue in Table 1). Considering the lessons learned from the initial qualification attempt, the second iteration of the qualification test vehicle for the basic HDI technology ("QTV2",Fig. 3) consists of a full panel design, including the following features.

- Test structures for HDI qualification test flow
  - A/B coupons including PTHs, core vias and microvias
  - ATC coupons including E, H and P coupon
  - TVX and SLX procurement IST coupons
- Coupons for outgoing inspection as detailed in clauses 8.2.2 and 8.2.3 of ECSS-Q-ST-70-60C
- BGA coupon which mimics (part of) an actual HDI PCB design
  - Functional and daisy-chain component fanout for 1.0 mm and 0.8 mm pitch component
    - CCGA, 1.0 mm pitch, 1752 I/Os (Xilinx Virtex 5QV FPGA)
    - CBGA, 0.8 mm pitch, 323 I/Os (Teledyne e2v EV12AQ600 ADC)
  - Routing to Axon Nano-D (1.27 mm) and Smiths connectors KVPX (1.35 mm)
- IPC D coupon including core vias and microvias
  - Coupon BHDI2-DPRO: propagated structures at 1.0 mm and 0.8 mm pitch
  - Coupon BHDI2-DBV: core vias at 1.0 mm and 0.8 mm pitch
  - Coupon BHDI2-DMVT: microvia stack at 1.0 mm and 0.8 mm pitch, top side
  - Coupon BHDI2-DMVB: microvia stack at 1.0 mm and 0.8 mm pitch, bottom side

The BGA coupon (Fig. 4) mimics (part of) an actual HDI PCB design and acts as "PCB" for the qualification test flow. The functional component fanout for 1.0 mm and 0.8 mm pitch components are based on the actual pinout diagrams for the Xilinx Virtex 5QV FPGA and the Teledyne e2v EV12AQ600 ADC, respectively. Controlled impedance differential pair routing was applied to all relevant output pins. As high-density connectors can impose restriction on routing and are thus also driving components for HDI, two candidates are included in the BGA coupon. The differential pair interconnections of the Xilinx Virtex 5QV FPGA component fanout are routed to eight KVPX connectors. The fanout of the Teledyne e2v EV12AQ600 is combined with the Axon nano-D connector.

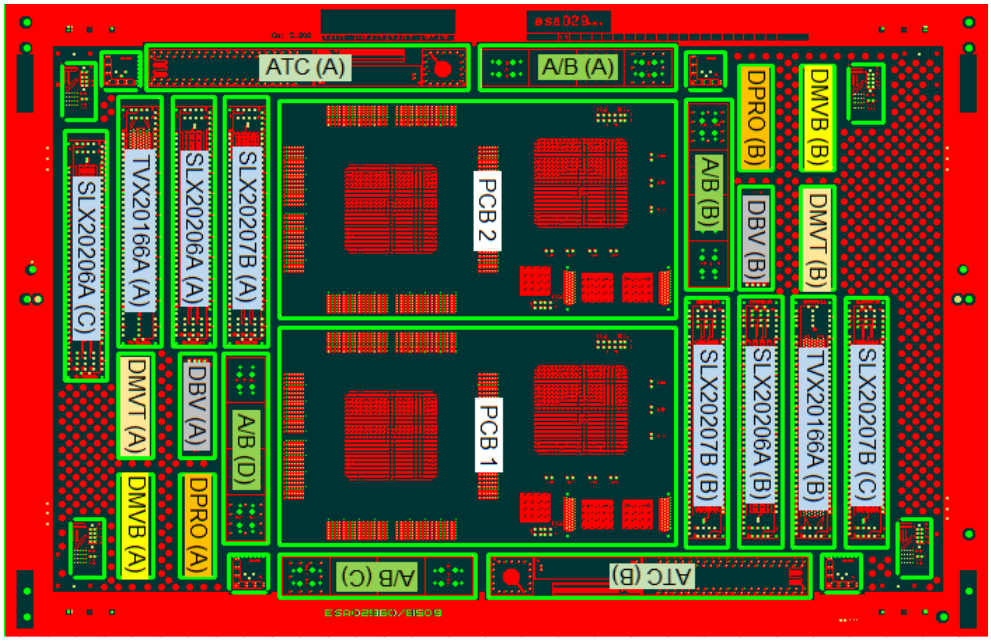

Fig. 3. Qualification Test Vehicle QTV2 with BGA coupons (*2x "PCB", centre of panel*), A/B coupons (*4x, surrounding the BGA coupons*), ATC coupons (*2x, surrounding the BGA coupons*), IST coupons (*2x or 3x three designs, surrounding the BGA coupons*) and D coupons (*2x four designs*)

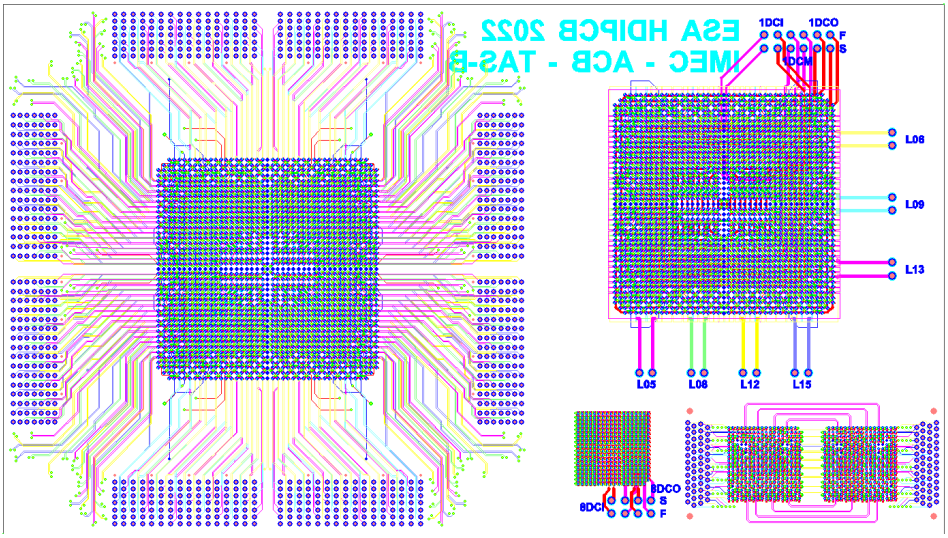

Fig. 4. BGA coupon with functional and daisy-chain component fanout for 1.0 mm and 0.8 mm pitch component and routing to high-density connectors (*ground layers removed for clarity*)

The electrochemical migration test vehicles for temperature-humidity-bias (THB) and CAF testing are produced on separate panels. The design and build-up of the THB test vehicle is in accordance with ECSS-Q-ST-70-60C [5]. For the initial qualification trials, a dedicated HDI CAF test vehicle was designed to better reflect the features and build-up of the qualification test vehicle. While the test results for the HDI CAF test campaign during the initial qualification were good, the revision of the basic HDI technology parameters required a repetition of the CAF testing as well as a redesign of the HDI CAF test vehicle. The main motivation for this was the increased drill diameter for the core vias, which at a constant pitch obviously results in a lower hole-wall-to-hole-wall spacing.

The HDI CAF test vehicle is designed to better represent HDI technology. It differs significantly from the ECSS CAF test vehicle that is required for qualification testing in accordance to ECSS-Q-ST-70-60C. All test structures on the ECSS CAF test vehicle use through-going vias at a fixed pitch of about 1.0 mm. The wall-to-wall distance is varied by changing the drill diameter. The lowest (inline) wall-to-wall distance (0.27 mm) is far below the lowest distance on the HDI CAF TV (0.45 mm for core vias) and even lower than the wall-to-wall distance of the microvia test structure (0.325 mm). The drill diameter for this distance is 0.8 mm, which is uncommon in HDI designs. For the HDI CAF TV, the mechanical drilling crosses four plated layers with higher copper thickness. No plated layers are present in the ECSS CAF TV at the time of drilling. Thicker copper layers can have an impact on the drill quality. Both CAF test vehicle designs have pros and cons. The outcome of the testing and the subsequent failure analysis will determine the merit of the new HDI CAF test vehicle design.

The qualification test flow is based on the ECSS-Q-ST-70-60C requirements for generic qualification of a HDI PCB. During testing, inspection and failure analysis, extra attention was paid to specific aspects related to HDI technology. These consist of the presence of microvias (aspect ratio, wrap copper requirement, interconnect defect), the presence of core vias (aspect ratio, filling, copper cracks), requirements for via plugging and cap plating, wicking and the fine-pitch line width and spacing. Table 2 shows an overview of the test results for the qualification test flow. The quality and performance of the microvias is excellent and the IST results for the core vias are a huge improvement over the previous qualification trial. Some non-conformances were found during the qualification test campaign. To address these, mitigations related to design, manufacturing and testing are proposed, as outlined in Table 3 and described below.

Table 2. Summary of test results for the HDI qualification of basic HDI technology

Group	**Test**	**Result** [(1)]
Group1	Visual inspection	OK
	Dimensional verification	OK
	Cleanliness	OK
	High resistance electrical test	OK
	Continuity test	OK
Group 2	Peel test	OK
Group 3	Microsectioning – as received	NOK
	Microsectioning – after thermal stress	OK
	IST	OK
Group 4	Insulation resistance – initial	OK
	Dielectric withstanding voltage – initial	OK
	Insulation resistance – after thermal cycling	OK
	Dielectric withstanding voltage – after thermal cycling	OK
	Peel test – after thermal cycling	OK
	Microsectioning – after thermal cycling	OK
Group 5	THB testing	OK
	CAF testing	NOK
Group 6	Microsectioning – after thermal cycling	NOK

[(1)] OK = no observations, OK = observation without non-conformance, NOK = non-conformance

Table 3. Overview of the recommendations related to design, manufacturing and testing for each of the non-conformances found during the qualification test campaign

Observation	**Design**	**Manufacturing**	**Testing**
MV annular ring	More representative coupon	None	DPA on PCB
Dielectric thickness	More representative coupon; Microvia layers as plane layers	Reduce target thickness for copper plating	DPA on PCB
Track width & spacing	None	None	DPA on PCB
Core via cracks	Reduced aspect ratio; Removal of NFPs; Material change	Increased Cu thickness; Use of plugging paste	Covered by IST; group 6 not needed
Inclusions (CAF)	None	Cleanliness of layup area	None

A DPA on PCB is recommended as an additional screening test for procurement. The intention is to inspect all via features (PTHs, core via and all microvias) as well as the copper and dielectric thickness, complementary to the coupon inspections. The microsection shall be performed once for each manufacturing batch, as these critical parameters can vary from batch to batch. This can be performed on a reject PCB. Multiple via features can be included in one microsection and both high-density areas (e.g. the AAD fanout) as well as isolated features relevant to the inspection are to be covered. Three microsections is considered a minimum to cover all required features. Thermal stress is not expected to impact the parameters to be inspected, so the inspection is performed in as-received condition.

A good match between the coupons and the PCB design remains a challenge for HDI technology. To ensure representativity, a part of the AAD footprint from the PCB design will be added as an additional coupon to each panel.

This AAD coupon should be kept small enough to fit in the periphery of the panel and not lose any PCB real estate. It shall be placed as close as possible to the PCB. The AAD coupon is inspected for each panel and as such covers panel to panel variation within a manufacturing batch. It is not considered an alternative to the abovementioned DPA on PCB, as the AAD coupon is located in the periphery of the panel. This difference in location can have an important impact on copper and dielectric thicknesses, for example. The inspection flow for this coupon should be consistent with the existing flow defined in ECSS-Q-ST-70-60C. Evaluation of acceptance criteria is performed in conformance with clause 10 of ECSS-Q-ST-70-60C, after three times thermal stress.

As-received microsectioning revealed that the dielectric thickness of the microvia layers was below the 60 µm requirement for the inner microvias in the A/B coupons and in the 1.0 mm pitch fanout on the PCB. This was caused by excessive copper thickness on the microvia layers (e.g. layer 3 in the left picture in Fig. 5). Copper balancing was not applied to the microvia layers of the BGA coupon design, which would help to increase the dielectric thickness in the PCB. Using microvia layers as plane layers and not as signal layers is a general design recommendation for HDI PCBs. Copper thickness requirements can differ from project to project. Designs with high power requirements will need a higher copper thickness, while for high-speed designs, the copper thickness should be kept low for controlled impedance routing. A certain thickness range could be added to the qualified domain, although this is not advisable. This range is dependent on the PCB design, making it difficult to provide a generic range. The use of thick copper (≥ 60 µm) is not needed for this technology and should be avoided.

Using thicker prepreg styles to increase the dielectric thickness is a risk, as it can lead to an unfavourable aspect ratio for the microvias. In comparison, the risk associated with a slightly reduced dielectric thickness is considered low. The prepreg construction for the microvia layers (2x 106) is defined in the qualified domain. This automatically limits the maximum copper thickness that can be allowed on microvia layers to ensure an as-manufactured minimum dielectric thickness of 60 µm. Following this reasoning, a higher base copper foil thickness (e.g. 17 µm instead of 12 µm) can be used as long as the total copper thickness is limited.

An important design restriction is the placement of the microvias with respect to the core via. For the design of the qualification test vehicle, superimposing the outer microvia above the core via was not allowed (Fig. 5). Partial or complete overlap was thus not evaluated during the qualification test flow and can as such not be considered qualified. The pad of the external microvia is to be placed tangent to the pad of the core via on the layer below, similar to the design rule for the internal microvia. This design rules still allows for various placement scenarios of the microvias: on a straight line with the core via, along the circumference of the core via pad, on opposite sides of the core via, etc. Not all of these configurations were evaluated in this qualification exercise, although there is no indication that they would not meet the qualification requirements.

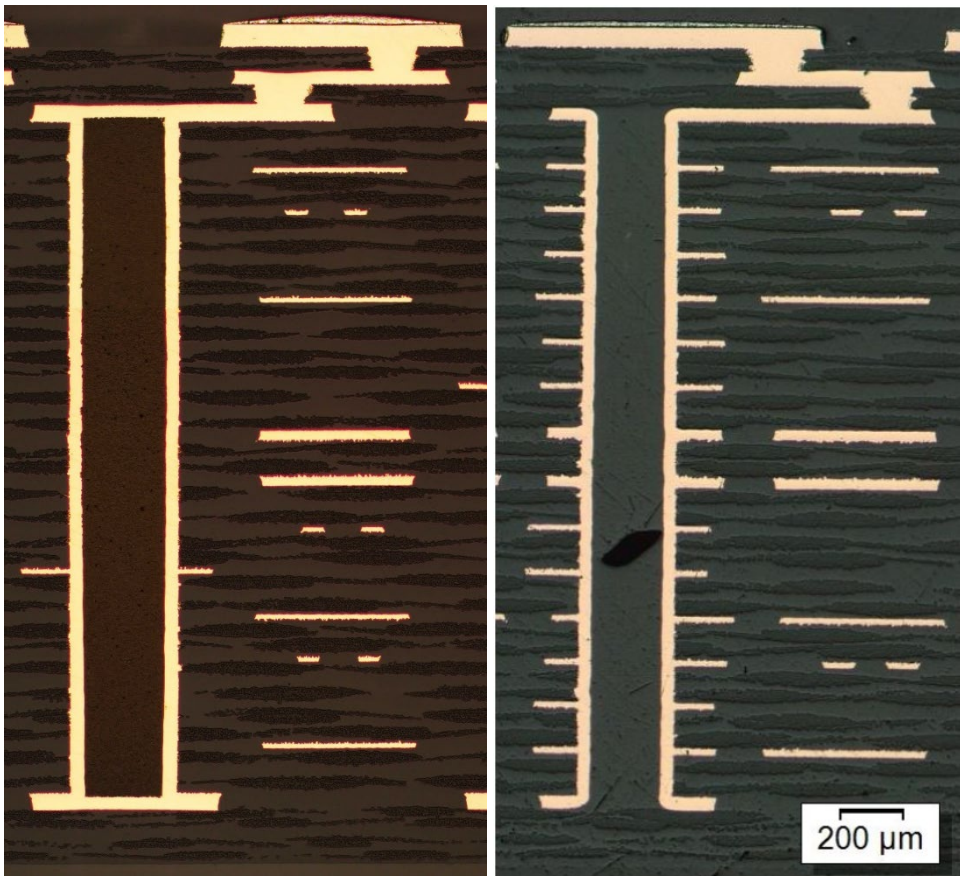

Fig. 5. Microsection of the 1.0 mm pitch fanout on the BGA coupon from QTV2 (350 µm core via, plugged and capped plated with NFPs removed, *left*), compared to the similar fanout on the BGA coupon from the initial QTV (300 µm core via, resin-filled with NFPs remaining, *right*)

The cracks in the copper plating of the core vias after group 4 and 6 testing is considered a low risk. The behaviour is well understood and the failure mode is covered by IST, for which the results were excellent [6]. Mitigations for design (reduced aspect ratio, removal of NFPs) and manufacturing (increased Cu plating thickness, use of plugging paste) are in place and have proven their merit. Fig. 5 shows these mitigations implemented on the a core via from the 1.0 mm pitch fanout on the BGA coupon from QTV2, compared to the fanout on the BGA coupon from the initial QTV.
CAF testing in group 5 produced a clear outcome and is considered a good test run. None of the defects found during CAF testing can be classified as conductive anodic filaments. The main cause for resistance drops during testing was the presence of inclusions in the form of foreign particles or contamination. The risk for CAF growth between core vias at a pitch of 0.8 mm and 1.0 mm (hole-wall-to-hole wall distance of 0.45 mm and 0.65 mm, respectively) is considered minimal. The inclusions found emphasize the need for continuous vigilance for cleanliness issues.

EVALUATION OF COMPLEX HDI TECHNOLOGY

Similar to the qualification test vehicle, the evaluation test vehicle (ETV, Fig. 6) consists of a full panel design, including the following features.

- Test structures for HDI qualification test flow
  - ATC coupons including A/B, E, H and P coupon
  - Coupon G for solder mask adhesion
  - Coupon W for solderability testing
  - TVX and SLX procurement IST coupons
- Coupons for outgoing inspection as detailed in clauses 8.2.2 and 8.2.3 of ECSS-Q-ST-70-60C
- BGA coupon which mimics (part of) an actual HDI PCB design
  - Functional component fanout for 1.0 mm, 0.8 mm and 0.5 mm pitch component
    - PBGA, 1.0 mm pitch, 2577 I/Os (Xilinx Virtex Ultrascale XCVU190 FPGA)
    - PBGA, 0.8 mm pitch, 896 I/Os (NXP QorIQ T2080 FPGA)
    - PBGA, 0.8 mm pitch, 321 I/Os (Teledyne e2v TD4GBDDR472 Memory)
    - PBGA, 0.5 mm pitch, 235 I/Os (Xilinx Artix-7 FPGA)
  - Routing to Smiths connectors KVPX (1.35 mm)
- Dedicated test coupons for the assessment of microvia test methods (D, HATS² single-via and CITC coupons)

The test results for the dedicated test coupons for the assessment of microvia test methods are reported in the respective section below on HDI reliability assessment.

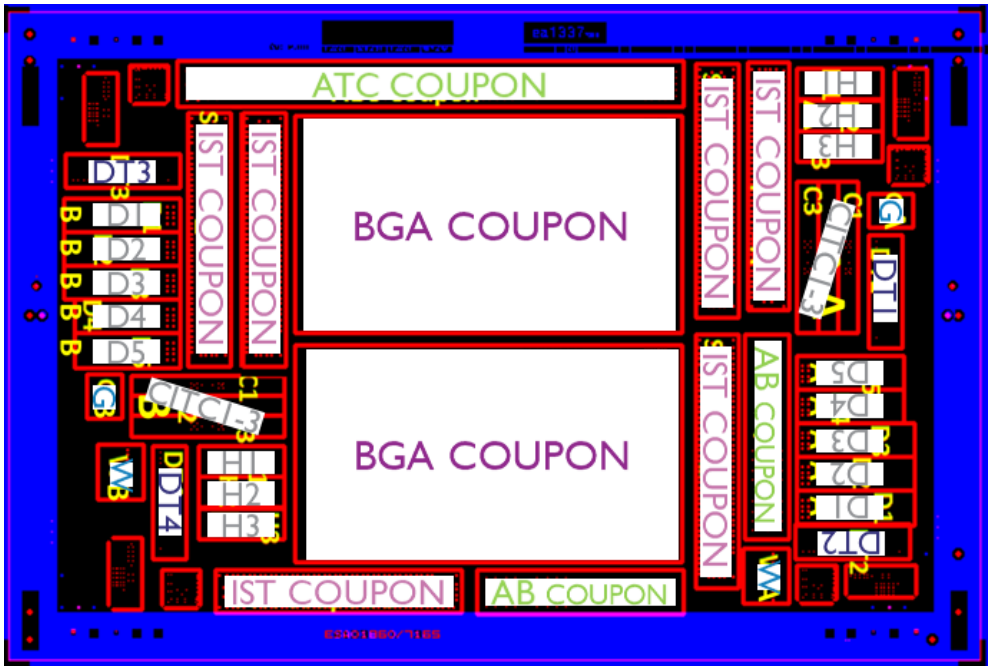

Fig. 6. Evaluation Test Vehicle with BGA coupons, test coupons for the qualification test flow (*ATC coupon, coupon G, coupon W and IST coupons*) and additional test structures (*D, HATS² and CITC coupons*)

The evaluation test vehicle is realized in both polyimide (Ventec VT-901) and high-speed material (Panasonic Megtron 6), using a similar 26-layer build-up (Fig. 7). The polyimide material is combined with an ENIG surface finish, while an ENEPIG surface finish is applied on the high-speed material. Note that the microvia layers consist of a single sheet of prepreg (1080 glass style for VT-901 and 1035 glass style for Megtron 6).

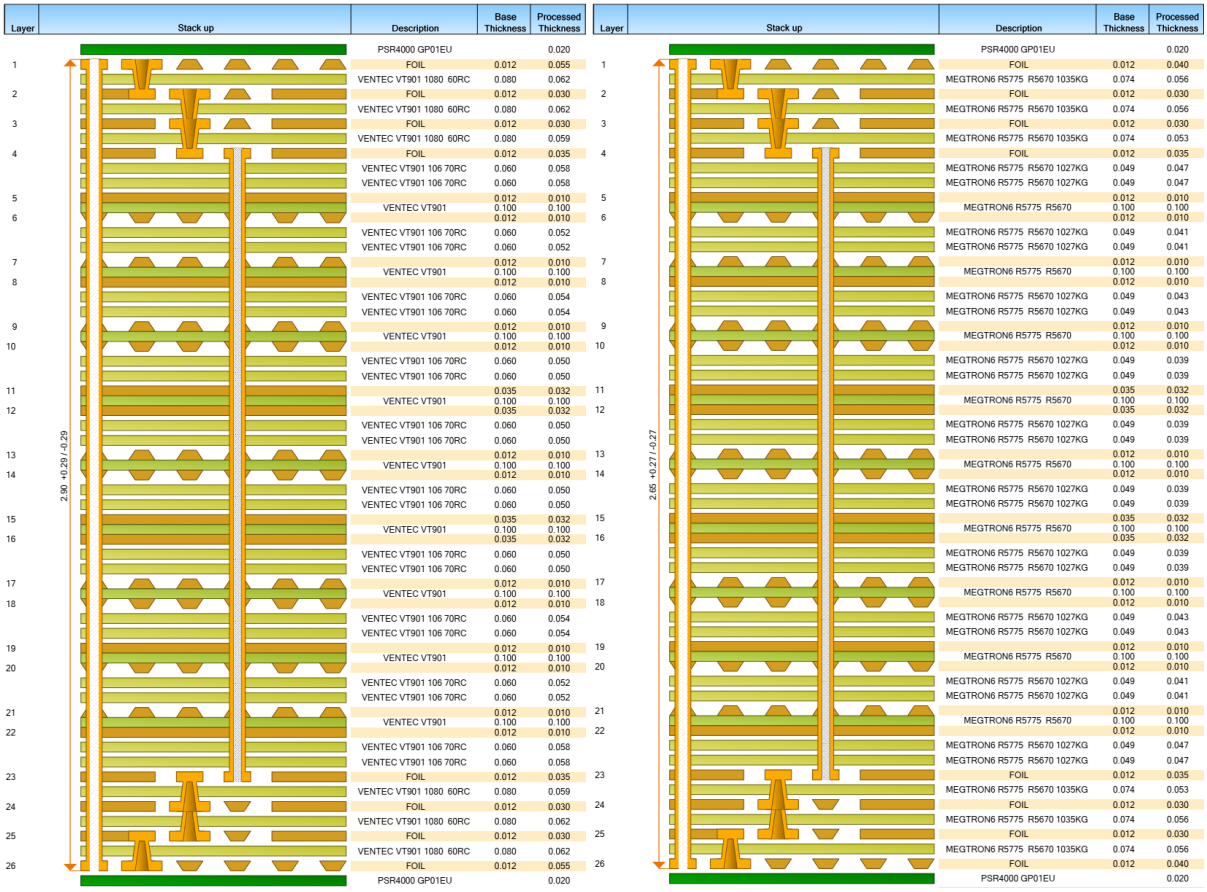

Fig. 7. Build-up for the ETV in Ventec VT-901 (*left*) and Panasonic Megtron 6 (*right*)

The BGA coupon again mimics (part of) an actual HDI PCB design and acts as “PCB” for the qualification test flow. The functional component fanout for 1.0 mm, 0.8 mm and 0.5 mm pitch components are based on the actual pinout diagrams for the Xilinx Virtex Ultrascale XCVU190 FPGA (2577 I/Os, 1.0 mm pitch), the NXP QorIQ T2080 FPGA (896 I/Os, 0.8 mm pitch), the Teledyne e2v TD4GBDDR472 DDR memory (321 I/Os, 0.8 mm pitch) and the Xilinx Artix-7 FPGA (235 I/Os, 0.5 mm pitch). These are all packaged in plastic ball grid arrays (PBGAs) and thus not space-qualified. The selected components represent potential future space-qualified packaging types. Controlled impedance differential pair routing is used for all relevant output pins. A non-solder mask defined approach is applied to the BGA pads, where the diameter of the opening in the solder mask is 100 µm wider than the pad diameter.

As a result of the single prepreg construction of the microvia layers, the microvia drill diameter can be reduced to 125 µm with a pad diameter of 275 µm. The drill diameter of the core vias for the complex HDI technology is lowered to 250 µm with a pad diameter of 550 µm. The semi-stacked inside microvia configuration was applied, consisting of two stacked microvias between layers 2 and 4 and a single, staggered microvia between layer 1 and 2. The latter cannot be placed superimposed to the core via. Design rule for microvia spacing as well as microvia-to-core via spacing is tangency of the pads. The stacked microvias are thus placed tangent to the core via. The outer, staggered microvia is located in between the core vias, tangent to the microvia stack. A microvia-in-pad design is used for the component pad.

One of the high-density connectors from the BGA coupon on the QTV, the Smiths connectors KVPX, was also included on the ETV-BGA design. The differential pair interconnections of the NXP QorIQ T2080 FPGA component fanout are routed to eight KVPX connectors.

The dedicated HDI CAF test vehicle designed for the basic HDI qualification was also used for the complex HDI evaluation. Since the testing was already completed for Ventec VT-901 during the basic HDI qualification and the HDI CAF TV design covers both basic and complex HDI design features, CAF testing is only performed for Panasonic Megtron 6. To match the twenty-layer design of the HDI CAF TV, a modified build-up is used including the 1027 glass style of the ETV core layers and the single sheet of 1035 prepreg for the microvia layers. An additional dummy lamination was performed before mechanical drilling of the through holes to represent the three levels of microvias. Surface finish is ENIG and the Megtron 6 material used for the HDI CAF TV is certified to Appendix A of IPC-4101.

The complex HDI technology introduces several new features, such as stacked microvias, via plugging , cap plating, solder mask and alternative surface finishes. Manufacturing risks and new failure modes are associated with each of these features. The goal of the evaluation test plan is to assess the performance of these features. This may lead to formal qualification for all or a subset of the technology features, depending on the occurrence of nonconformances in the evaluation. The test methodology aims at decoupling the risks associated with these features as much as possible. This not only increases the overall chance of success but allows achieving qualifications status where successful.

The test flow for evaluation of the complex HDI technology is based on the ECSS-Q-ST-70-60C requirements for generic qualification of an HDI PCB. The test methods and the number of samples are in accordance with ECSS-Q-ST-70-60C, except for the solder mask adhesion and the solderability testing. These features are evaluated using the test methods specified in IPC-6012ES, the space addendum to IPC-6012E [7].
It should be noted that the manufacturing and testing of the ETV was completed before the qualification of the revised basic HDI technology. Lessons learnt from the initial basic HDI qualification trial were applied to the complex HDI evaluation. The recommendations from the revised basic HDI qualification, however, were not.
Table 4 shows an overview of the test results for the evaluation test flow for both materials. While the test campaign on Ventec VT-901 polyimide can be considered relatively successful, a number of non-conformances were observed during testing. Solderability testing using a wetting balance did not meet the requirements of IPC-4552 [8]. This was also the case for the ENEPIG finish on Megtron 6. The full evaluation and eventual qualification of the ENIG surface finish is further pursuit outside of this project.

Table 4. Summary of test results for Ventec VT-901 polyimide and Panasonic Megtron 6 RF material

Group	Test	VT-901	Megtron 6
Group1	Visual inspection	NOK	OK
	Dimensional verification	OK	OK
	Cleanliness	OK	OK
	High resistance electrical test	OK	OK
	Continuity test	OK	OK
Group 2	Coating adhesion	OK	OK
	Solder mask adhesion	OK	OK
	Solderability	NOK	NOK
	Outgassing	N/A	OK
	Thermal analysis	N/A	OK
Group 3	Microsectioning – as received	OK	NOK
	Microsectioning – after thermal stress	OK	NOK
	IST	NOK	OK
Group 4	Insulation resistance – initial	OK	OK
	Dielectric withstanding voltage – initial	OK	OK
	Insulation resistance – after thermal cycling	OK	OK
	Dielectric withstanding voltage – after thermal cycling	OK	OK
	Peel test – after thermal cycling	OK	OK
	Microsectioning – after thermal cycling	NOK	NOK
Group 5	CAF testing	N/A	NOK
Group 6	Microsectioning – after thermal cycling	NOK	NOK

(1) OK = no observations, OK = observation without non-conformance, NOK = non-conformance

The core vias in Ventec VT-901 did not reach the required IST endurance of 400 cycles. Furthermore, copper cracks are observed after group 4 and group 6 testing. While the IST results for Megtron 6 were acceptable, copper cracks are also observed after both group 4 and group 6 testing. The recommendation of plating additional copper inside the core via was not yet implemented at the time of the manufacturing of the ETV samples. As concluded after the basic HDI qualification, the phenomenon of cracks in the copper plating of the core vias after group 4 and 6 testing is well understood. Mitigations for design (reduced aspect ratio, removal of NFPs) and manufacturing (increased Cu plating thickness) from the basic HDI technology can be implemented for the complex HDI technology as well. Reducing the aspect ratio by increasing the drill diameter of the core vias will, however, come at a cost of reduced routing density for the fanout of 0.5-0.8 mm pitch AAD.
A large variation in dielectric thickness between the different fanouts is observed on every layer for both materials (Fig. 8). Even within one fanout on the same layer there are large difference observed, despite the fact that all microvia layers on the BGA coupon were completely filled with copper. This is likely caused by the lower amount of resin in the single sheet of prepreg, combined with the flow behaviour of that resin. While the minimum thicknesses of 50 µm on Ventec VT-901 and 55 µm on Megtron 6 are not considered critical, the large variation in dielectric thickness can have an impact on microvia processing and thus reliability. Furthermore, the strong variation makes it difficult to draw conclusions with respect to the acceptance criteria for minimum dielectric thickness, annular ring for microvias and contact diameter on the target pad.

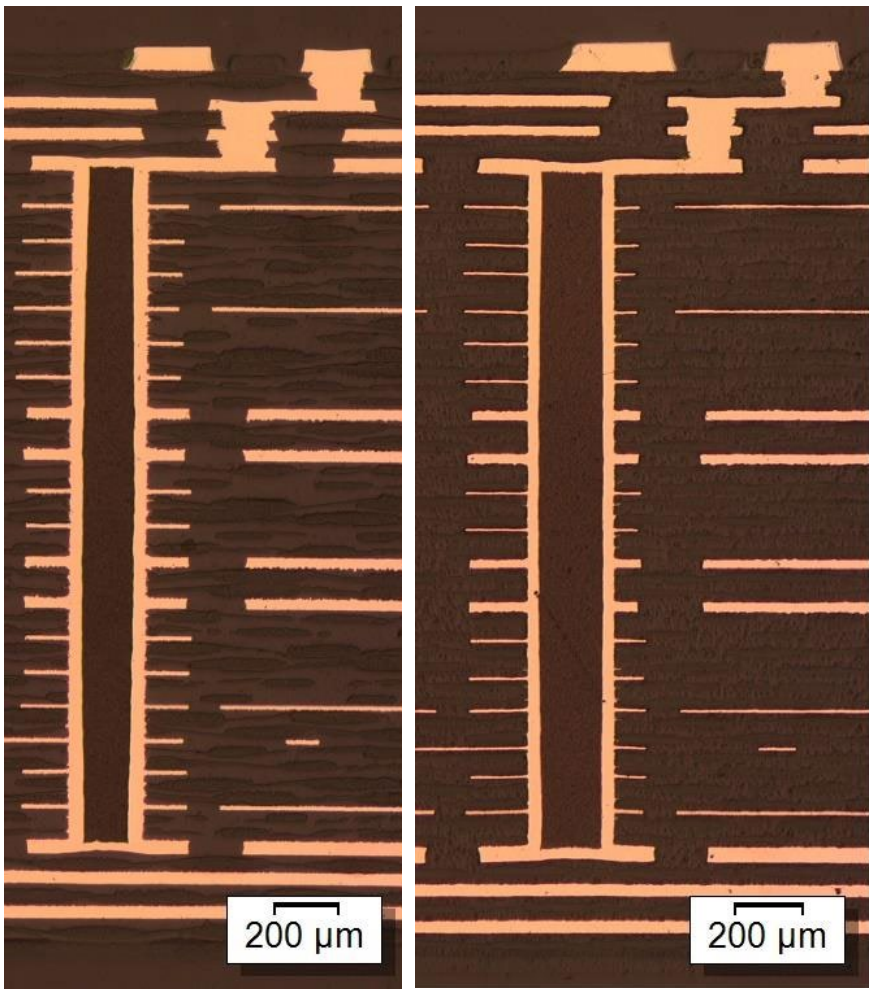

Fig. 8. Microsection of the 0.5 mm pitch fanout on the BGA coupon from ETV (250 µm core via, plugged and capped plated with NFPs remaining) in Ventec VT-901 polyimide (*left*) and Panasonic Megtron 6 high-speed material (*right*)

Wicking is a very important parameter for HDI technology as it can potentially reduce the insulation distance between the via and a neighbouring conductor or plane. Excessive wicking also increases the risk for CAF growth. The measured wicking is slightly above the requirement of 25 µm for both materials, but still well below the minimum annular ring measured after manufacturing (> 65 µm, see Fig. 8). It should be noted that tweaking of the drilling parameters to further reduce the wicking could have adverse effects in other areas.
Taking into account the recommendations above, the non-conformances for the complex HDI in Ventec VT-901 can be overcome and a qualification of the technology should be within reach.
After group 4 and group 6 testing of Megtron 6, dielectric cracks are observed above and below the core vias, in resin-rich areas surrounding the microvias and also near the end points of the solder mask. The dielectric cracks and their criticality are to be judged from a helicopter view. Even if some of the observed cracks are not considered critical, the multiple occurrences of dielectric cracks suggest a propensity of the material to cracking and is flagged as an unacceptable risk. While some of the non-conformances for Panasonic Megtron 6 could be resolved with the recommendations proposed for the Ventec VT-901 polyimide, the multiple occurrences of dielectric cracks are considered a showstopper.

HDI RELIABILITY ASSESSMENT

Interconnect stress testing

The goal of the IST benchmarking round robin study was twofold: to set a baseline for HDI technology at the ESA-qualified PCB manufacturers and to evaluate the updated IST test methodology for HDI PCBs. IST coupon designs for testing microvias and core vias were procured from all ESA-qualified PCB manufacturers at the time. Based on the outcome of the testing, the coupon design approach and the test parameters for both core vias and microvias are believed to be sound. The lack of microvia failures is both reassuring and unsatisfactory. No failures after 6x preconditioning to 230 °C followed by 1000 cycles to 210 °C proves that the manufacturing quality of microvias from these space-qualified PCB manufacturers is high. The positive results, however, do not permit to determine an undisputable acceptance criteria and IST endurance threshold for microvias, apart from the criteria already specified in ECSS. The strong variation in thermal cycles to failures for the core vias allows to analyse the results in more detail. Three contributing factors are observed to have a relevant impact on the results: the thickness of the plated copper inside the core via, the CTE of the

base material and the behaviour of the resin inside the core via. The influence of these factors in IST and the potential difference in failure mechanism during traditional chamber thermal cycling is further investigated below. More details about the IST benchmarking can be found in [6].
IST prescreening of the complex HDI technology was the second IST study, performed to evaluate the semi-stacked microvia configurations "semi-stacked outside" (SSO, two-stack at the outside) and "semi-stacked inside" (SSI, two-stack at the inside), with the latter slightly outperforming the former. The goal of the third and final IST study was to evaluate different approaches for non-functional pad (NFP) removal on core vias. Removing non-functional pads has several benefits such as more space for routing, improved signal integrity, improved yield and quality as drill wear is reduced. Based on the results and the failure analysis, it can be concluded that removing non-functional pads increases the IST performance of core vias. The results for alternative configurations illustrated that non-functional pads act as a stress riser and thus removing all non-functional pads gives the best IST performance. It should be noted that this IST study evaluates the risk of removing non-functional pads on core vias only. The results cannot be expanded to through-going vias or component holes. Manual soldering operations could lead to higher stress on these types of vias.

Microvia test methodology

Microvia technology has been used in production since the 1990s. In the beginning, the design freedom for HDI PCBs was only limited by the imagination of the designer, resulting in very ambitious constructions. It became apparent quickly that there are limitations on how many microvias one can stack on top of each other and where to place them with respect to the core via. Since product acceptance testing is time constrained, microvia testing is often performed at elevated stress levels that do not directly equate to product life. The aim of testing is to assert the manufacturing quality of the microvia, under the assumption that a properly manufactured microvia will not negatively impact the reliability of the product.
An extensive test campaign has been executed, covering three levels of microvias in three different materials (high-Tg FR4, high-speed material and polyimide). The build-up and design rules for the microvia study are based on the complex HDI technology parameters. In this study, four accelerated test methods were combined with six different microvia configurations (Fig. 9). Fully stacked, fully staggered and semi-stacked microvia configurations were assessed. For the fully staggered and semi-stacked configuration, the influence of the location of the core via was investigated. The applied test methods consist of convection reflow assembly simulation followed by air-to-air thermal shock on daisy chained D-coupon, reflow assembly simulation followed by thermal shock on HATS² single-via coupon, interconnection stress testing (IST) and current-induced thermal cycling (CITC). The results revealed both excellent performance of stacked microvias as well as the possibility of the test methods to detect weaknesses in design, material or manufacturing.
This microvia test methodology evaluation cannot be separated from the weak microvia interface issues that plagued the high-reliability industry in recent years. Microvias can fail for the following reasons: non-optimised materials or processes, stressful design and inhomogeneous processes. A weakness in the microvia target land interface is not caused by any single manufacturing process. For his reason, ESA recommends to evaluate microvia designs using review of design and comparison to qualification, perform thermo-mechanical modelling, test coupons and spare PCBs and review manufacturing processes. To support the latter, a document with microvia process guidelines was drafted by PCB experts and specialists from chemistry suppliers [9].

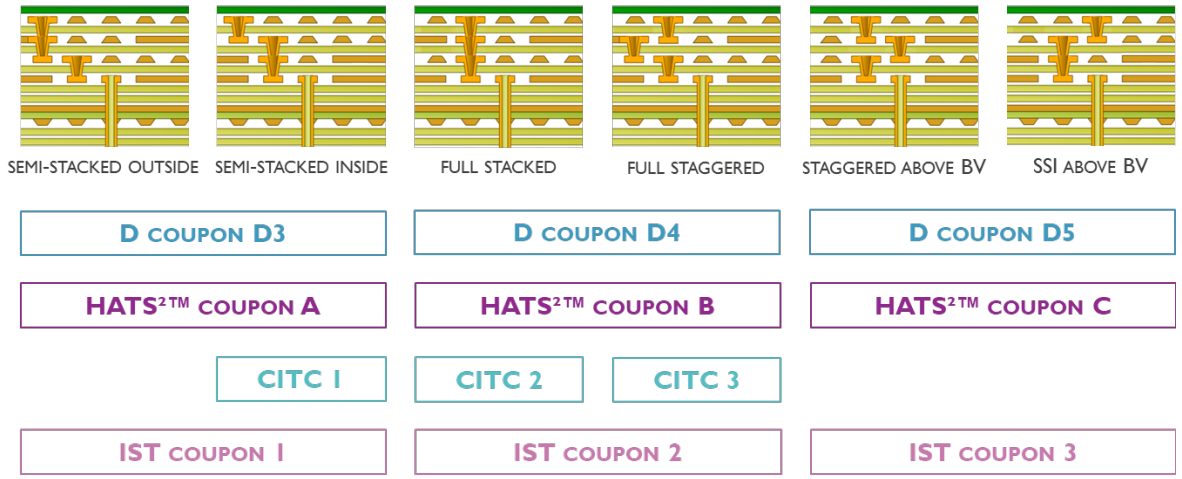

Fig. 9. Overview of the microvia configurations included per coupon design (*BV = buried via*)

The various test campaigns did not provide new insights but rather confirmed the known principles of microvia testing. All microvia configurations investigated in this study can be considered reliable, if designed carefully, manufactured properly and assembly is performed with caution. Under these conditions, even three levels of stacked microvias should not reduce the reliability of the HDI PCB. Robustness testing at elevated temperatures can be used to differentiate between microvia configurations. The outcome of these tests needs to be assessed carefully, as even the worst performers in robustness testing can be sufficiently reliable for the intended end application.

The dominant failure mechanism for microvias remains interface separation. This failure mechanism is not automatically an indication of a weak interface, as the highest strain levels are found near the base of the microvia. Coincidently, this is also where the most precarious interfaces are located: the base copper to the electroless copper and between the electroless copper and the electrolytic flash plating. Assuming no manufacturing or other defects are present at or near these interfaces, cracks tend to propagate from the circumference of the microvia base towards the centre of the target pad. This holds true for two and three levels of stacked microvias. Cycling of stacked microvias at moderate temperatures below or near Tg, as opposed to reflow temperatures, did reveal crack initiation at the fibre bundles close to the centre of the via structure. This more resembles the fatigue behaviour of mechanical vias and is consistent with the higher overall length of the taller stacked microvia structures.
Fig. 10 illustrates the impact of design factors, such as the distance between the core via and the microvia stack, on microvia reliability. Within a microvia stack, the thermal stress on individual microvias is higher when they are placed closer together (①). On the other hand, tightly spaced microvia stacks (i.e. small pitch) act as rivets, reducing stress on each stack [10]. The low-CTE plugging paste inside the core via restricts the movement of that core via (②). How this affects microvias is the subject of further investigation, although it is assumed that it can result in rotational stress on nearby microvias. The presence of copper planes on the microvia layers determines the amount of resin-rich volume below the microvia which increases stress on the microvia (③). Concentric placement of staggered microvia to the core via reduces rotational stress compared to partial super positioning (④). Similarly, the inhomogeneous presence of planes below the microvia increases rotational stress.

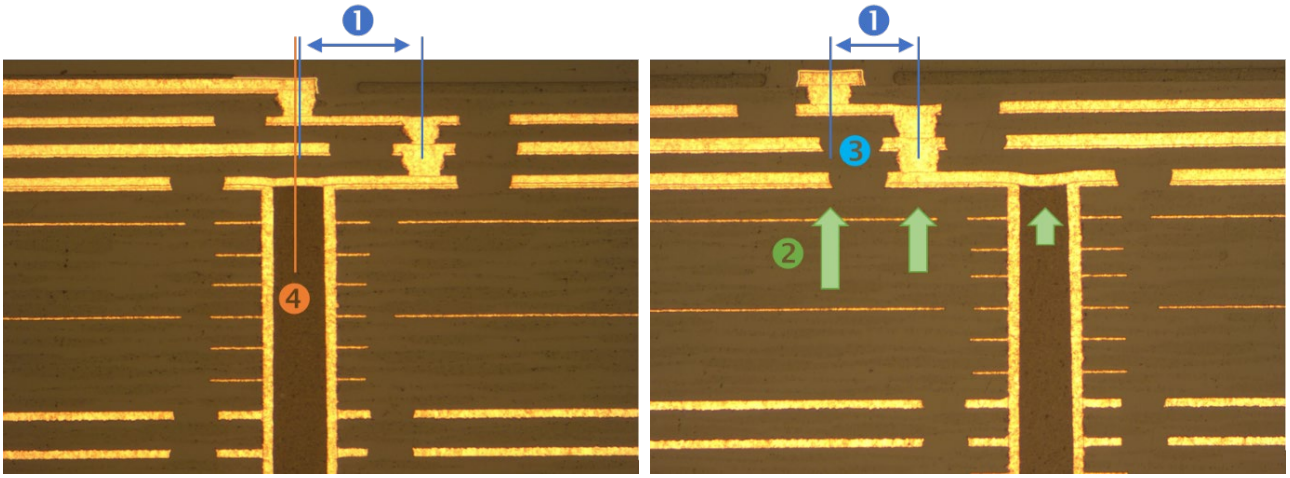

Fig. 10. Design factors affecting microvia reliability: distance between microvias ①, distance to core via ②, copper-resin distribution ③, and super positioning of staggered microvia to core via ④

As most test houses agree, there is no single, ideal test method to evaluate microvias. All test methods apply elevated stress levels to assess the quality of the microvia. Comparing results between test methods is precarious, even under well-controlled circumstances. Experience is key in evaluating test results. Test houses with decades of test results are still learning every day. A thorough understanding of the impact of design variables, manufacturing processes and test parameters is more important than the choice of a microvia test method.

Core via reliability

The cornerstone of HDI PCB technology is the combination of microvias and core (or buried) vias, which provide a significant increase in routing density. Microvias have received a lot of attention in recent years due to the well-known weak interface issues. Looking at the hierarchy of failure, the core via is expected to fail before the (properly manufactured) microvia and the larger diameter plated through-hole (PTH). The reliability of the core via is determined by several contributing factors: design parameters such as via pitch, drill diameter, aspect ratio, material choice and presence of non-functional pads in combination with manufacturing variables such as plated copper thickness inside the core via and the use of plugging paste (Fig. 11).
Lessons learnt for through-going vias or PTHs are often translated to core vias, while failure mechanisms can differ significantly. An important difference is the presence of material inside the core via, which can be prepreg resin from adjacent layers or a dedicated plugging paste. This material exerts force from the inside of the barrel, resulting in crack growth from the inside towards the outside of the core via. In combination with the crack growth in the opposite direction, this results in earlier failure compared to a PTH of the same dimensions.

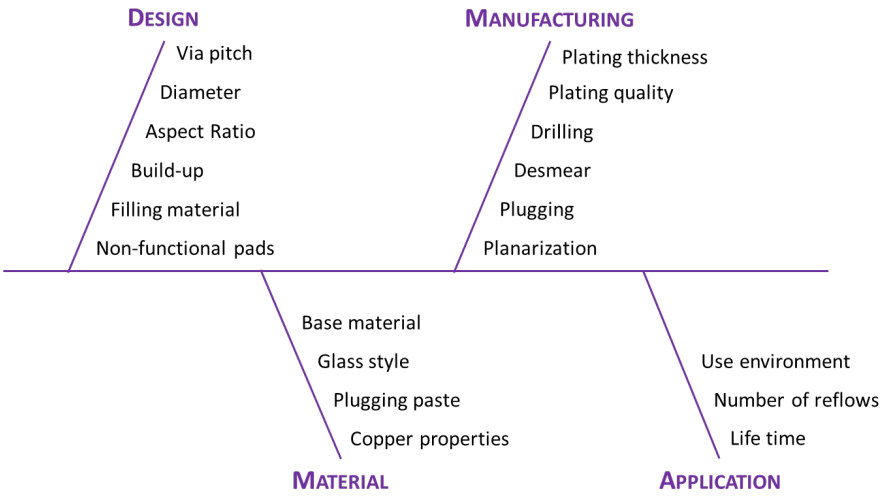

Fig. 11. Contributing factors to core via reliability

The following contributing factors to core via reliability were investigated in more detail. Test parameters for various test methods such as chamber thermal cycling, interconnection stress testing or air-to-air thermal shock highlight the impact of these contributing factors. Observations from several test campaigns are corroborated with finite element method (FEM) modelling to better understand the respective failure mechanisms. More details can be found in [11].

- **Core via pitch**: Although the positive influence of reducing the pitch might feel counterintuitive, it can be explained by the amount of base material surrounding the core via. When the drill diameter remains constant, reducing the pitch results in less base material in between the core vias. While the expansion of the material remains the same, the relative force exerted by the material on the core via is reduced. In addition, each via is supported by the close proximity of adjacent vias that all act as rivets and limit the material movement.
- **Core via diameter and aspect ratio**: The number of cycles to failure more or less increase linear with the drill diameter. Reducing the drill diameter obviously changes the aspect ratio of the core via. A higher aspect ratio typically makes it more challenging to manufacture the core via, especially with respect to obtaining the required plated copper thickness inside the core via. When comparing two drill diameters while keeping the aspect ratio constant, the largest diameter still outperforms the smaller diameter. The smaller diameter via itself comprises a lower cross-sectional area of copper. As such, it is a lower modulus feature, easier strained by the material expansion. As third effect, its surrounding vias are also weaker, again increasing the effect of material movement.
- **Plated copper thickness**: As mentioned above, an important difference between plated through-holes and core vias is the presence of material inside the core via. The thermal expansion of this material exerts a force from the inside of the copper barrel, resulting in crack initiation when the strain becomes sufficiently high. The endurance of a core via thus depends on the interaction of three materials: the base material surrounding the core via, the plated copper inside and the material inside the core via. Changing the pitch, drill diameter or copper thickness of the core vias influences the relative contribution of the three materials. Consequently, the IST endurance increases exponentially with increasing copper thickness at a constant drill diameter and pitch.
- **Base material**: HDI PCBs use thin laminate and prepreg layers in their construction, which are provided with relatively high overall resin content. Regardless of the resin system, HDI constructions with thin glass fibre styles exhibit a higher thermal expansion in Z-direction. For unfilled polyimide resin systems, the impact of switching to a high-resin content HDI construction on the overall CTEz was observed to be significant. Furthermore, typical for unfilled polyimide base materials, the CTE below Tg strongly depends on temperature.
- **Plugging paste**: In case the prepreg resin from the microvia layers is used to fill the core via, the observations regarding the thermal expansion of the base material are also relevant for the material inside the core via. In addition, the material inside of the core via is expanding isotropic ($CTE_{X-Y} = CTE_Z$). The combined movement in X-Y and Z direction of the highly expanding resin inside the core via leads to stress concentration around the via pads (Fig. 12). This can result in a rotational effect, consistent with the crack locations observed on the coupons after testing. Thicker copper makes the barrel more robust and less susceptible to the rotational forces. Plugging paste can reduce the thermal expansion inside the core via, but the CTE difference with the base material should not be too high in order to avoid excessive shear stress. Next to the manufacturing challenges of filling a core via with plugging paste and potential cap plating, selecting a suitable plugging paste can be critical to core via reliability. A common guideline is to match the thermomechanical properties (CTE, Tg and modulus) of the plugging paste with the base material. For filled resin systems with moderate expansion in Z direction (40 – 60 ppm/°C below Tg), the CTE difference with the plugging paste will remain low. The high levels of expansion for polyimide HDI constructions combined with a low CTE plugging paste can lead to excessive shear stress, resulting in hole wall pull away and interconnect defects. If the adhesion of the copper to both the plugging paste and the base material is good, the large difference in CTE results in additional stress on the copper and again a reduced thermal reliability.

- **Presence of non-functional pads**: A dedicated test campaign to assess the impact of removing non-functional pad was performed as part of the IST evaluation of specific aspects of the complex HDI technology (see above). Based on that test campaign, it can be concluded that removing non-functional pads increases the IST endurance of core vias. Non-functional pads act as a stress riser and thus removing all non-functional pads gives the best IST performance.

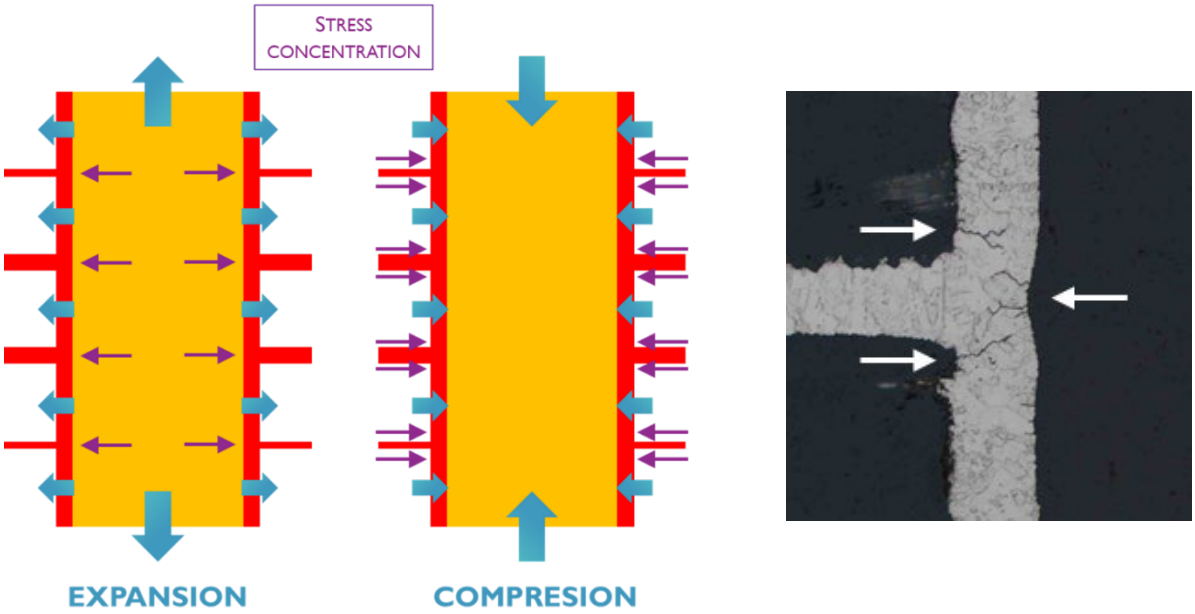

Fig. 12. Locations of stress concentration (*purple*) during thermal expansion and compression in case of isotropic expansion of the resin inside the core via. Right picture shows crack locations above, below and opposite the pad

Each of the contributing factors described above has a relative impact on the IST endurance of a core via. Note that we talk about IST endurance rather than reliability, as many recommendations are derived from IST. In most cases, a higher IST endurance translates into better reliability. Some contributing factors, however, might have a stronger impact on IST endurance than on core via reliability.
Core via reliability can be improved by increasing the drill diameter, depositing more copper inside the core via, removing the non-functional pads and selecting the right plugging paste. The endurance of a core via depends on the interaction of three materials: the base material surrounding the core via, the plated copper and the material inside the core via. The lower the pitch, the higher the impact of the material inside the core via and the higher the riveting effect from adjacent vias. Selecting an appropriate plugging paste requires knowledge of the dominant failure mode and compromises might need to be made to obtain the required endurance.
The conclusions and recommendations in this study related to core via reliability are predominantly based on test results for polyimide HDI constructions. As with so many other PCB-related topics, it is not possible to make general claims or to extrapolate these results to other situations. Each contributing factor should be assessed separately considering the design, construction, material combinations and mission profile.

Conductive anodic filaments

Electrochemical migration (ECM) failures result in a drop in insulation resistance between neighbouring structures, which can lead to catastrophic failure of the electronic system. External ECM failures on PCBs are typically related to surface contamination and manufacturing residues. ECM failures internal to the board can be related to cleanliness issues (inclusions of foreign materials), material deficiencies (weak polymer resin bond, hollow fibres, laminate cracks) or conductive anodic filament (CAF) growth. External and internal cleanliness issues as a result of base material contamination or manufacturing residues are evaluated using Temperature, Humidity, Bias (THB) testing (clause 9.7.2 of ECSS-Q-ST-70-60C). The test method and the associated ECSS THB test vehicle design cover the requirements for HDI PCBs.
CAF propensity depends on the material, the PCB manufacturing processes and the design. It is important that the resin of the material is completely wetting the woven glass reinforcement and that the adhesion between glass and resin is intimate and not easily weakened by moisture. Drilling cracks and wicking are initiation points for CAF and these features need to meet the workmanship requirements and be representative of the process flow of the PCB manufacturer. The design determines the insulation distances of key features such as vias, tracks and planes. The decreasing pitch of the driving components for HDI technology results in a reduction in spacing between the vias used in the component fanout. This reduction of the hole wall to hole wall distance increases the risk for CAF growth. In addition, large matrices of tightly spaced vias are a challenge for defect-free manufacturing.

The CAF testing was performed in accordance with clause 9.7.2 of ECSS-Q-ST-70-60C in a CTS CS-40/200 climate chamber using a Gen3 Systems Auto-SIR 256 with a 256-channel test rack. Three test campaigns were executed in the project as part of the initial basic HDI qualification, the complex HDI qualification and the revised basic HDI qualification. The basic HDI campaigns evaluated the Ventec VT-901 polyimide material, while the complex HDI CAF test campaign only covered the Panasonic Megtron 6 high-speed material. The revision of the basic HDI technology parameters required a redesign of the HDI CAF test vehicle. The main motivation for this was the increased drill diameter for the core vias, which at a constant pitch obviously results in a lower hole-wall-to-hole-wall spacing. Consistent with the QTV numbering, the CAF test vehicles are referred to as HDI CAF TV and HDI CAF TV2.
Overall, the CAF test campaigns seem to be sound with a credible outcome. An overview of the number of failures per test structure for all three test campaigns is provided in Table 11. Every test structure is tested 30 times, since each test campaign consisted of 10 samples. For the core vias, the results are split over the two HDI CAF TV designs. No failures were observed on the test structures with PTHs. One microvia test structure out of 30 showed a drop in insulation resistance near the end of the test. This momentary drop is not believed to be related to ECM or CAF. Core via failures are scattered among the test structures with failures occurring much more frequent for a pitch of 0.8 mm. Three out of four failures for test structure A1-1 occurred on samples from the same panel. The large majority of failures, however, is observed on the via-to-plane test structures (C1-5).

Table 5. Overview of the CAF test results per test structure for all three test campaigns (*last two columns provide the # failed per material*)

ID[1]	Pitch	Via	Type	Fibers	W-W/W-P	# tested	# failed	VT-901	Megtron 6
A7	0.5	Microvia	Inline	both	0.325 mm	30	1	1	0
A1-1	0.8	Core via	Inline	warp	0.50 mm	20	4	4	0
A1-2	0.8	Core via	Inline	warp	0.45 mm	10	0	0	-
A4-1	0.8	Core via	Inline	weft	0.50 mm	20	0	0	0
A4-2	0.8	Core via	Inline	weft	0.45 mm	10	0	0	-
B1-1	0.8	Core via	Diagonal	warp	0.707 mm	20	1	1	0
B1-2	0.8	Core via	Diagonal	warp	0.636 mm	10	0	0	-
B3-1	0.8	Core via	Diagonal	weft	0.707 mm	20	1	1	0
B3-2	0.8	Core via	Diagonal	weft	0.636 mm	10	1	1	-
A2-1	1.0	Core via	Inline	warp	0.70 mm	20	0	0	0
A2-2	1.0	Core via	Inline	warp	0.65 mm	10	0	0	-
A5-1	1.0	Core via	Inline	weft	0.70 mm	20	0	0	0
A5-2	1.0	Core via	Inline	weft	0.65 mm	10	0	0	-
B2-1	1.0	Core via	Diagonal	warp	0.990 mm	20	0	0	0
B2-2	1.0	Core via	Diagonal	warp	0.919 mm	10	1	1	-
A3	1.27	PTH	Inline	warp	0.77 mm	30	0	0	0
A6	1.27	PTH	Inline	weft	0.77 mm	30	0	0	0
C1	1.27	Core via	Via to plane	(both)	0.225 mm	30	1	1	0
C2	1.27	Core via	Via to plane	(both)	0.200 mm	30	3	1	2
C3	1.27	PTH	Via to plane	(both)	0.225 mm	30	12	8	4
C4	1.27	PTH	Via to plane	(both)	0.200 mm	30	12	9	3
C5	1.27	PTH	Via to plane	(both)	0.250 mm	10	3	3	-

Notes: 1. Suffix 1 refers to HDI CAF TV and suffix 2 refers to HDI CAF TV2. Structure C5 only present on HDI CAF TV2

The combination of reduced insulation distances and the increased number of closely-spaced mechanical vias means there is an increased risk for CAF in HDI PCBs. The testing performed in this project on a dedicated HDI CAF TV did, however, not reveal actual CAF growth. The majority of failures could be linked to the presence of contaminations, suggesting that cleanliness remains the bigger concern. This observation also triggers the discussion on the added value of a dedicated HDI CAF test vehicle. While the design and build-up are more representative for HDI PCBs, more manufacturing resources are required and the testing and failure analysis become more complex. Extending the ECSS CAF TV design to a non-sequential build-up with representative glass styles and higher layer count could offer a reasonable compromise.

CONCLUSION

Six years ago, a three-year project was started with the ambitious goal of developing and qualifying high-density interconnect PCBs for space applications. Based on the thorough understanding of the requirements for HDI PCBs, the

manufacturing capability and associated reliability was evaluated using a dedicated test methodology. The HDI technology parameters for the basic and complex HDI technology, defined in cooperation with relevant stakeholders, were translated into several test vehicle designs that were submitted for qualification or dedicated evaluation test campaigns. This paper presents an overview of the most important findings and learnings from this interesting journey.
ESA qualification for high density interconnect printed circuit boards was granted to PCB manufacturer ACB in Belgium, based on the basic HDI technology parameters. The non-conformances for the complex HDI in Ventec VT-901 can be overcome and a qualification of the technology should be within reach. The relevance of the complex HDI technology for advanced components with additional data speed and power requirements, however, appears diminished.
Following the weak microvia interface issues, the recommended aspect ratio for high-quality microvias is 0.66 to 0.75. Both the dielectric thickness and the base copper foil thickness need to be considered for the calculation of the microvia aspect ratio. To minimize variations in dielectric thickness, the microvia layers should be assigned as plane layers. This also ensures the best control over the plated copper thickness. Even three levels of stacked microvias can be considered reliable, if designed carefully, manufactured properly and assembly is performed with caution.
The endurance of a core via depends on the interaction of three materials: the base material surrounding the core via, the plated copper and the material inside the core via. Changing the pitch, drill diameter or copper thickness of the core vias influences the relative contribution of the three materials. The contributing factors, ranked from largest to smallest relative contribution, are: increasing the copper thickness from 25 µm to 35 µm; changing the base material; increasing the drill diameter and reducing the pitch from 1.0 mm to 0.8 mm. Reducing the pitch can, however, have a negative impact on solder joint reliability.
The combination of reduced insulation distances and the increased number of closely-spaced mechanical vias means there is an increased risk for CAF in HDI PCBs. The testing performed in this project on a dedicated HDI CAF TV did, however, not reveal actual CAF growth. The majority of failures could be linked to the presence of contaminations. Cleanliness thus remains critical for HDI PCBs. This applies to both the base material as well as the manufacturing processes, most notably the layup before lamination.

REFERENCES

[1] M. McCurdy, I. de Sousa, R. Martel and A. Lessard, "CGA Trends and Capabilities," *SMTA International 2015 Proceedings*, Rosemont, IL, 2015.
[2] B. Schafsteller, G. Ramos, M. Rosin, and T. Schlosser, "ENIG Corrosion - When It Gets Critical and How Is the Status in the PCB Industry?," *SMTA International 2020 Proceedings*, 2020 (online).
[3] B. Gumpert, W. Fox., C. Don Dupriest, "Evaluation of the Use of ENEPIG in Small Solder Joints in Thermal Cycling," *SMTA International 2016 Proceedings*, Rosemont, IL, 2016.
[4] ECSS-Q-ST-70-12C (14/07/2014) – Design rules for printed circuit boards, available online at www.escies.org.
[5] ECSS-Q-ST-70-60C Corrigendum 1 (01/03/2019) – PCB qualification and procurement, available online at www.escies.org.
[6] M. Cauwe, C. Nawghane A. Coulon, M. Van De Slyeke, and, S. Heltzel, "Contributing factors to the reliability of buried vias in high-density interconnect PCBs," *Proceedings of the 23rd IPC APEX EXPO*, San Diego, CA, 2023.
[7] IPC-6012ES (Jan 2020) – Space and Military Avionics Applications Addendum to IPC-6012E, Qualification and Performance Specification for Rigid Printed Boards
[8] IPC-4552A (08/01/2017) – Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Boards
[9] ESA-TECMSP-TN-19672 (18/11/2020) – Microvia process guidelines.
[10] Partida, G., "Next Progression in Microvia Reliability Validation – Reflow Simulation of a PCB Design Attributes and Material Structural Properties at Design," *Proceedings of the 22nd IPC APEX EXPO*, San Diego, CA, 2022.
[11] M. Cauwe, S. Heltzel, J. Furlong, C. Nawghane, M. Van De Slyeke, and A. Coulon, "Round robin testing of HDI technology from space-qualified PCB manufacturers," *Proceedings of the 21st IPC APEX EXPO*, 2021 (online).